**2-input gates using 2:1 mux**

**Definition of a multiplexer**: A 2^n-input mux has n select lines. It can be used to implement logic functions by implementing LUT (Look-Up Table) for that function. A 2-input mux can implement any 2-input function, a 4-input mux can implement any 3-input, an 8-input mux can implement any 4-input function, and so on. This property of muxes makes FPGAs implement programmable hardware with the help of LUT muxes. In this post, we will be discussing the implementation of 2-input AND, OR, NAND, NOR, XOR and XNOR gates using a 2-input mux.

**2-input AND gate implementation using 2:1 mux**: Figure 1 below shows the truth table of a 2-input AND gate. If we observe carefully, OUT equals '0' when A is '0'. And OUT follows B when A is '1'. So, if we connect A to the select pin of a 2:1 mux, AND gate will be implemented if we connect D0 to '0' and D1 to 'B'.

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| [A 2-input AND gate has output '0' when either or both inputs is '0'. And output is '1' when both the inputs are '1'.](https://4.bp.blogspot.com/-0O658SRzBgA/V26DOoWZwYI/AAAAAAAAAcY/oMICO0SYYxgdeSwdQ_uHk_nMOU4zvmU0QCK4B/s1600/and%2Bgate%2Btruth%2Btable.png) |
| **Figure 1: Truth table of AND gate** |

Figure 2 below shows the implementation of 2-input AND gate using a 2:1 multiplexer.

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| [An AND gate can be implemented using a 2-input multiplexer by connected D0 input to '0' and D1 to B, SEL being connected to A. AND gate using mux, AND gate using 2x1 mux, 2-input AND gate using mux](https://2.bp.blogspot.com/-wpdUgS69Iwg/V26FMgwTVlI/AAAAAAAAAck/uExKp-QTkRstWiyhiaCU4VAVU0itJ7QygCK4B/s1600/and%2Bgate%2Busing%2Bmux.png) |
| **Figure 2: Implementation of AND gate using a 2:1 mux** |

**2-input NAND gate using 2:1 mux**: Figure 3 below shows the truth table of a 2-input NAND gate. If we observe carefully, OUT equals '1' when A is '0'. Similarly, when A is '1', OUT is B'. So, if we connect SEL pin of mux to A, D0 pin of mux to '1' and D1 to B', then it will act as a NAND gate.

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| [In a 2-input NAND gate, output is '0' when both inputs are '1', otherwise output is '1'](https://1.bp.blogspot.com/-4hX601Qv4FU/V26Fk1SplzI/AAAAAAAAAcs/SP3W0Gi5_DIgZqKZJF59wqlxGrvtfdV2ACK4B/s1600/nand%2Bgate%2Btruth%2Btable.png) |
| **Figure 3: Truth table of 2-input NAND gate** |

Figure 4 below shows the implementation of a 2-input NAND gate using 2:1 mux.

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| [A NAND gate can be implemented using a 2-input multiplexer, if we connect the select pin of the multiplexer to A, D0 to VDD and D1 to B' inputs. NAND gate using mux, NAND gate using 2x1 mux](https://4.bp.blogspot.com/-RMy4afET4do/V26GWiBZx0I/AAAAAAAAAc4/W2N2g4OmKcwMMbLAQ4m3LVTk9U9FvrdpACK4B/s1600/nand%2Bgate%2Busing%2Bmux.png) |
| **Figure 4: Implementation of 2-input NAND gate using 2:1 mux** |

**2-input OR gate using 2x1 mux**: Figure 5 below shows the truth table for a 2-input OR gate. If we observe carefully, OUT equals B when A is '0'. Similarly, OUT is '1' (or A), when A is '1'. So, we can make a 2:1 mux act like a 2-input OR gate, if we connect D0 pin to B and D1 pin to A, with select connected to A.

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| [In a 2-input OR gate, output is '1' when either or both of the inputs are '1'. Otherwise, output is '0'.](https://3.bp.blogspot.com/-6vRlDRurZpg/V26JYj7Qn2I/AAAAAAAAAdI/2AmR7tG0W2wV2Nw70J2vu3UcBTk4lsWMACK4B/s1600/or%2Bgate%2Btruth%2Btable.png) |
| **Figure 5: Truth table of 2-input OR gate** |

Figure 6 below shows the implementation of 2-input OR gate using a 2:1 multilpexer:

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| [A 2-inputs multiplexer can be converted to an OR gate, if we connect the select pin of mux to A-input, D0 to B-input and D1 to VDD. OR gate using mux, OR gate using 2x1 mux](https://1.bp.blogspot.com/-5UGczWwAJ6A/V26KCuyW8oI/AAAAAAAAAdQ/i0YhE939t9QFUacOeFBKGcL1xY5722kaACK4B/s1600/or%2Bgate%2Busing%2Bmux.png) |
| **Figure 6: Implementation of 2-input OR gate using 2:1 mux** |

**2-input NOR gate using 2x1 mux**: Figure 7 below shows the truth table of a 2-input NOR gate. If we observe carefully, OUT equal B' when A is '0'. Similarly, OUT equals '0' when A is '1'. So, we can make a 2-input mux act like a 2-input NOR gate, if we connect SEL of mux to A, D0 to B' and D1 to '0'.

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| [In a 2-input NOR gate, output equals '0' when either or both the inputs is '1'. Otherwise, output is '0'.](https://2.bp.blogspot.com/-YJMwIbe1abQ/V26Q6hC3WlI/AAAAAAAAAdk/cTx2cxffZi0ADnoYZNp3Fk_zLkITBWeRACK4B/s1600/nor%2Bgate%2Btruth%2Btable.png) |
| **Figure 7: Truth table of 2-input NOR gate** |

Figure 8 shows the implementation of 2-input NOR gate using 2:1 mux.

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| [NOR gate using mux, 2-input NOR gate using 2:1 mux, NOR gate using 2x1 mux](https://1.bp.blogspot.com/-kQtDySygB6s/V26Rvu4WnAI/AAAAAAAAAdw/9R4x5BQgsyYHMmdxuwriFozC3YdZrKtJACK4B/s1600/nor%2Bgate%2Busing%2Bmux.png) |
| **Figure 8: Implementation of 2-input NOR gate using 2x1 mux** |

**2-input XNOR gate using 2x1 mux**: Figure 9 below shows the truth table of a 2-input XNOR gate. If we observe carefully, OUT equals B' when A is '0' and equals B when A is '1'. So, a 2-input XNOR gate can be implemented from a 2x1 mux, if we connect SEL pin to A, D0 to B' and D1 to B.

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| [In a 2-input XNOR gate, output equals '0' when exactly one of the inputs is '1', otherwise output is '1'.](https://4.bp.blogspot.com/-tGpd6mrkesg/V26SxcdG0KI/AAAAAAAAAd8/1lR66Wg2lEQHT8r10aIIkqLxBdZuYd8_gCK4B/s1600/xor%2Bgate%2Busing%2Bmux.png) |
| **Figure 9: Truth table of 2-input XNOR gate** |

The implementation of 2-input XOR gate using a 2x1 mux is as shown in figure 10.

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| [A 2-input XNOR gate can be realized using a 2:1 mux provided we connect the select to A-input, D0 to B' and D1 to B. XNOR gate using mux, XNOR gate using 2x1 mux, 2-input XNOR gate using mux](https://2.bp.blogspot.com/-pIfdi876xE8/V26gXRwgUBI/AAAAAAAAAeU/V6qxrgnZCJ8jnzzXwvvq8dO7tZRmo52OQCK4B/s1600/xnor%2Busing%2Bmux.png) |
| **Figure 10: Implementation of 2-input XNOR gate using 2x1 mux** |

**2-input XOR gate using 2x1 mux**: Figure 11 shows the truth table for a 2-input XOR gate. If we observe carefully, OUT equals B when A is '0' and B' when A is '1'. So, a 2:1 mux can be used to implement 2-input XOR gate if we connect SEL to A, D0 to B and D1 to B'.

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| [In a 2-input XNOR gate, output equals '1' when exactly one of the inputs is '1', otherwise output is '0'.](https://4.bp.blogspot.com/-wV0mZuUK7v4/V26gvK_7zdI/AAAAAAAAAec/ZA4VgCvseHIf_oRJsW5kGonWfdGfrJMWQCK4B/s1600/xor%2Bgate%2Btruth%2Btable.png) |
| **Figure 11: Truth table of 2-input XOR gate** |

Figure 12 shows the implementation of 2-input XOR gate using 2x1 mux.

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| [A 2-input XNOR gate can be realized using a 2:1 mux provided we connect the select to A-input, D0 to B and D1 to B'. XOR gate using mux, 2-input XNOR gate using mux, XNOR gate using 2:1 mux](https://1.bp.blogspot.com/-GCYJLI2aAwo/V26hYC-0I8I/AAAAAAAAAes/_FAaVWxdQJsi0wPKAZhx2AC9ZlNibsb5QCK4B/s1600/xor%2Bgate%2Busing%2Bmux.png) |
| **Implementation of 2-input XOR gate using 2x1 mux** |

**NOT gate using 2:1 mux**: Figure 13 shows the truth table for a NOT gate. The only inverting path in a multiplexer is from select to output. To implement NOT gate with the help of a mux, we just need to enable this inverting path. This will happen if we connect D0 to '1' and D1 to '0'.

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| [Truth table of NOT gate](https://2.bp.blogspot.com/-mERXdrcLy0k/WCCUmEj_ZII/AAAAAAAAAzI/z5cOX0y84dwtYBz4tgGHz4Qmns9QJDKKQCK4B/s1600/NOT%2Btruth%2Btable.png) |
| **Figure 13: Truth table of NOT gate** |

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| Figure 14 shows the implementation of NOT gate using 2x1 mux:  [NOT gate using 2-input mux, NOT gate using mux, NOT gate using multiplexer](https://1.bp.blogspot.com/-GL-kW_W3Muk/WcZ9WkB0TYI/AAAAAAAABBY/2irA1J7hbowpWWYGWeGKZl_R_KxWWW0MgCLcBGAs/s1600/not_using_mux.png) |
| **Figure 14: Implementation of NOT gate using 2x1 mux** |